



Siemens S5 Series

Overview

Maple Systems' MAP Family & OIT Family Operator Interface Terminals (Maple OITs) communicate with Siemens SIMATIC S5 Series and Westinghouse 500 Series of Programmable Logic Controllers (PLCs) using the Loader Port protocol.

Compatible PLCs	
PLC Family	PLC Model
Siemens SIMATIC S5 Series	S5-95U, S5-100U, S5-115U
Westinghouse 500 Series	PC50, PC55, PC500, PC502, PC503

Communications Cable

Any information regarding to the Siemens SIMATIC S5 Series PLCs covered in this document also applies to the Westinghouse 500 Series PLCs except where specifically noted.

The Maple OIT should be connected to the communication port of the programmable logic controller. Since this is a current loop communications port, the connection to the OIT must be made using a RS232 to current loop converter (Siemens P/N 6ES5 966-0AA22 or Westinghouse P/N NLCC-3100). The cable/converter unit converts the PLC's current loop interface to RS232, which then connects to the Maple OIT's serial port.

Refer to Technical Note 1061 for information on communication cable part numbers and cable assembly instructions. If you will be assembling your own communications cable, cable assembly instructions are also available on our web site at www.maple-systems.com.

WARNING: If your communications cable is not wired exactly as shown in our cable assembly instructions, damage to the Maple OIT or loss of communications can result.

PLC Settings

It is important to connect the OIT to the PLC's communications port correctly using a current-loop to RS232 interface cable converter which can be purchased from the manufacturer of the PLC.

Accessible PLC Memory

PLC Register Memory

The following table lists the PLC register memory ranges that Maple's OITs are able to access. Please note that your PLC's memory range may be *smaller* or *larger* than that supported by Maple's OITs. The following PLC register memory is displayable in 16-bit or 32-bit formats on the Maple OIT.

PLC Register Address	PLC Register Description
AI0.0 to AI15.3	Analog Input Channels
AQ0.0 to AQ15.3	Analog Output Channels
SD0.0 to SD255.15	System Data/Status Coils and Registers
T0 to T127	Timer Register Present (Accumulated) Values
C0 to C127	Counter Register Present (Accumulated) Values
DW2:0 to DW255:255	User Data Registers

PLC Discrete Memory

The following table lists the PLC discrete memory ranges that Maple's OITs are able to access. Please note that your PLC's memory range may be *smaller* or *larger* than that supported by Maple's OITs. The following discrete PLC memory is displayable in single-bit and bank formats on the Maple OIT.

PLC Bit Address	PLC Bit Description
I0.0 to I127.7	Digital Input Coils
Q0.0 to Q127.7	Digital Output Coils
F0.0 to F255.7	Flag Coils

OITware-200 Settings

The following table lists the communications settings that must be configured in OITware-200.

Please note:

- the Default column lists OITware-200's default setting; your PLC's default may be different
- the Options column lists OITware-200's options; your PLC may not support every option

Name	Default	Options	Important Notes
Baud Rate	9600	19200, 9600, 4800, 2400, 1200, 600, 300	Must match the PLC port settings. Use the fastest baud rate supported by both.
Parity	Even	Even, Odd, None, Mark, Space	Must match the PLC port settings.
Data Bits	8	7, 8	Must match the PLC port settings.
Stop Bits	1	1, 2	Must match the PLC port settings.
Status Coils	F200	F0 to F255	Must be within the PLC's supported memory range.
Address, Source Address, Destination Address	N/A		
Password	N/A		
Message Request Register	DB2:DW0	DB2:DW0 to DB255:DW255	Must be within the PLC's supported memory range.
Current Message Register (optional)	DB3:DW232	DB2:DW0 to DB255:DW255	Must be within the PLC's supported memory range.
Function Key Coils (optional)	F202	F0 to F255	Must be within the PLC's supported memory range.
Screen Dependent Function Key Coils (optional)	F204	F0 to F255	Must be within the PLC's supported memory range. Applies to OITs with Screen Dependent Function Keys.
Control Key Coils (optional)	F205	F0 to F255	Must be within the PLC's supported memory range.
Status LED Coils (optional)	F0	F0 to F255	Must be within the PLC's supported memory range. Applies to OITs with Status LEDs.
Function Key LED Coils (optional)	F203	F0 to F255	Must be within the PLC's supported memory range. Applies to OITs with Function Key LEDs.

MAPware-100 Settings

The following table lists the communications settings that must be configured in MAPware-100. Please note:

- the Default column lists MAPware-100's default setting; your PLC's default may be different
- the Options column lists MAPware-100's options; your PLC may not support every option

Name	Default	Options	Important Notes
Baud Rate	9600	19200, 9600, 4800, 2400, 1200, 600, 300	Must match the PLC port settings. Use the fastest baud rate supported by both.
Parity	Even	Even, Odd, None, Mark, Space	Must match the PLC port settings.
Data Bits	8	7, 8	Must match the PLC port settings.
Stop Bits	1	1, 2	Must match the PLC port settings.
Status Coils	F200	F0 to F255	Must be within the PLC's supported memory range.
Address, Source Address, Destination Address	N/A		
Password	N/A		
Message Request Register	DB2:DW0	DB2:DW0 to DB255:DW255	Must be within the PLC's supported memory range.
Function Key Coils (optional)	F202	F0 to F255	Must be within the PLC's supported memory range.

Important PLC Memory Considerations

If your PLC's memory range is smaller than the range supported by Maple's OITs, it is possible to configure the Maple OIT to monitor a PLC memory address which does not exist. Since this can cause unpredictable results, when you configure the Maple OIT please ensure that all selected PLC memory addresses are valid for your PLC model.

Do not configure the Maple OIT to write to any PLC memory address which should only be written to by the PLC.

Using the Data Block (DW2:0-255:255) Registers

The D (User Data) register addresses reflect the data block and word address of the PLC. The number to the left of the colon is the block number and the number to the right of the colon represents the word address within the data block. Therefore, address DW4:201 corresponds to data block 4, word register 201. If the OIT tries to read a data block that has not been created in the PLC program then the OIT will generate an error, *OIT ADDRESS TABLE FAULT*. Before the OIT can read or write to any data block register in the PLC, the PLC programmer must create the data block using the PLC programming software. Data blocks DW0 and DW1 cannot be accessed by the OIT since these data blocks are used by the PLC for system data.

On using Bank 8 or Bank 16 formats

When using these formats, each PLC coil (bit) is individually displayed in terms of 1 and 0, with the lowest addressed coil displayed in the right-most position in the field. Therefore, if using coils Q0.0-Q1.7, then Q0.0 is the least significant bit displayed in the right-most position and Q1.7 is the most significant bit displayed in the left-most position.

Using the Digital Inputs (I) and Outputs (Q)

The I (Digital Input) and Q (Digital Output) addresses reflect the slot and coil of the PLC's PII (Process Input Image) and PIQ (Process Output Image). When monitoring the digital input (I) coils using the OIT, the register monitor should be configured as read only since the PLC does not allow these inputs to be written to.

Using the Timer (T) and Counter (C) registers

The timer and counter data registers of the PLC store the current or accumulated value of the timer/counter. However, the current value is stored in the nine least significant bits of the register in decimal format (0-999). The six most significant bits are used for other purposes such as recording the time base used for the timer. Therefore, in order for the OIT to accurately read the current time or count, the contents of the timer/counter should be moved to a data block register (DW). The OIT can then be programmed to monitor the data block register using decimal format. Because of the format used for the timer/counter registers by the PLC, these registers should not be directly written to by the OIT.

Using the Analog Inputs (AI) and Outputs (AQ)

The AI (Analog Input) and AQ (Analog Output) addresses reflect the slot and channel of the PLC's PII (Process Input Image) and PIQ (Process Output Image). An address of AI0.0 corresponds to IW64 in the PII, while AI0.1 corresponds to IW66, etc. The AQ addresses corresponds to the PIQ in a similar manner. Each analog slot takes up four channels or eight bytes of the PII and PIQ tables. Therefore, address AI1.1 is Slot 1 Channel 1 of the Analog Input registers, which is located in the PII table at address IW74. Similarly, address AQ5.3 is Slot 5 Channel 3 of the Analog Output registers which is located in the PIQ Table at address QW110. Analog Inputs are stored in the process image input table (PII) in the following manner:

	High Byte								Low Byte							
Bit number	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Analog Value	S	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	X	E	OV

S = Sign bit 0 = "+" 1 = "-"

X = Irrelevant bits

E = Error bits 0 = no wire break, 1 = wire break

OV = Overflow bit 1 if +/-4096

In order to read the actual value presently stored in the analog input, the OIT should be programmed to monitor the register using signed format with linear scaling. The linear scaling formula should be $Y = 1/8X+0$.

Analog Outputs are stored in the process image output table (PIQ) in the following manner:

	High Byte								Low Byte							
Bit number	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Analog Value	S	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	X	X	X	X

S = Sign bit 0 = "+" 1 = "-"

X = Irrelevant bits

OV = Overflow bit 1 if +/-2048

In order to read the actual value presently stored in the analog input, the OIT should be programmed to monitor the register using signed format with linear scaling. The linear scaling formula should be $Y = 1/16X+0$.