TECHNICAL NOTE

Model	Title	TN7010
HMC3000 Series HMC7000 Series HMC2000 Series HMC4000 Series MLC Series PLC MAPware-7000 P/N: 0907-7010 Rev. 04 Date: 10/12/2022	High Speed Counters and Encoders	

Summary

Many control processes require the use of an encoder for precision measurement of motion. This technical note covers the interactions of the HMC products with high speed counters and encoders.

Solution

The HMC products offer High Speed Counters (HSC) on several I/O modules. These counters offer support for a single channel pulse train (single input) or multi-channel for use with quadrature encoders (multi-input). Note that not all models support every mode of operation. Consult the specifications for the particular model being used.

Modes:

Single Phase up Counter

This mode is used to count the number of incoming pulses to a digital input (X). The pulse count is increased by 1 each time a new pulse is received on the input. The accumulated count is compared to a preset value- when the values match; a predefined configuration bit (M) is set. There is also an option to set a physical output (Y). Once the accumulated value reaches the preset value, a configuration bit (M) or physical input (X) can be used to reset the accumulated value back to 0. A configuration bit (M) is used to enable or disable the counter.

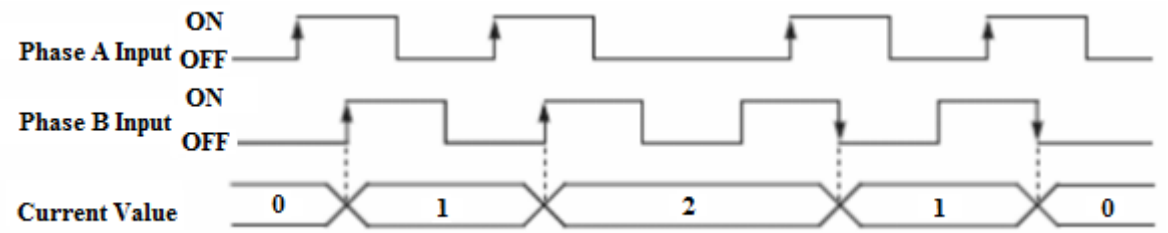
Single Phase down Counter

This mode is similar to the Up-Counter described above, except that the accumulated value starts at 4,294,967,295 and counts down to the preset value. For models that support both Phase Up and Phase

Down counting, direction is controlled by a second digital input (X). When the input is high, the counter will count up. When it is low, the counter will count down

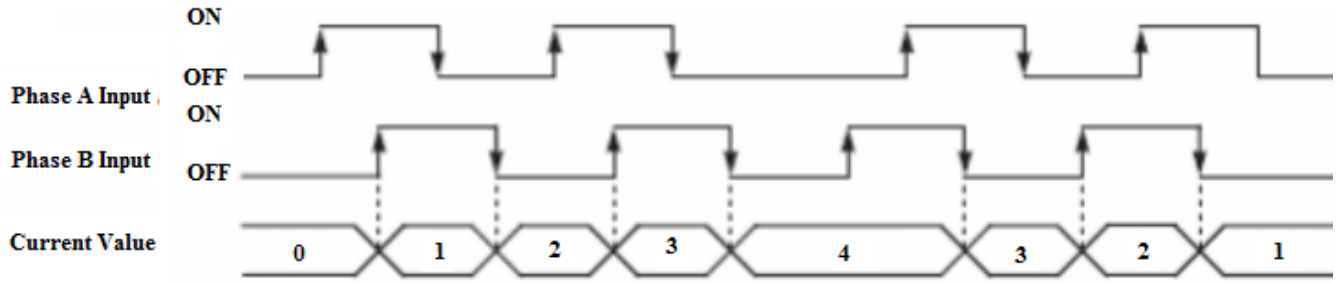
Quadrature 1X Mode

Quadrature encoders are used to measure the speed and direction (clockwise or counter-clockwise) of a device. Each encoder has two tracks, A and B (thus two inputs are required), that are 90° out of phase, which enable it to provide accurate position information. It will count up when phase A precedes, and count down when phase B precedes. The length of travel can be determined by the speed of the incoming pulses. With 1X mode, the current value increments or decrements at the rising or falling edge of the phase B input after the phase A input has turned on.



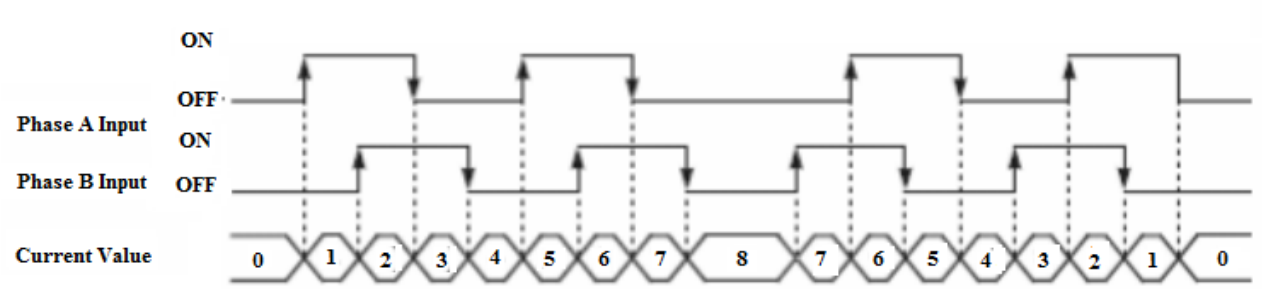
Quadrature 2X Mode

Quadrature 2X Mode works the same as 1X Mode, except that the current value increments or decrements at the rising or falling edge of the phase B input after the phase A input has turned on or off.



Quadrature 4X Mode

Quadrature 4X Mode works the same as 1X and 2X Modes, except that the current value increments or decrements at the rising or falling edges of the phase A and B inputs. Both rising and falling edges of each phase are counted. This essentially quadruples the number of pulses per revolution, by counting 4 times the pulse frequency.



HMC3000 High Speed Counters

The HMC3000 Series modules have built-in High-Speed counters that link directly to specific inputs and outputs. Specific registers and bits are predefined for setup and control of these counters. No logic is required to run the counters, other than logic that may be used for configuration and control.

Two inputs on the module are used as the Triggers for the High-Speed counters, and two outputs are used as the done bits. The inputs support a maximum speed of 200 KHz.

Implementation of HSC on HMC3000 Series

1. Connect a device that will provide the high-speed pulses to one of the high-speed inputs on the expansion module.
2. Configure the HSC using the configuration register for that channel. Note: You can write to the configuration register value using the Power-Up logic block or in a Power-Up Task.
3. Write the HSC preset count value in that channel's Preset Register.
4. Enable the HSC by setting the HSC Enable Bit for that channel.
5. HSC increments the current value register for that channel until the preset value is reached.
6. Enable the HSC Reset Bit for that channel. This will cause the HSC current value to reset back to 0.
7. To start the process again, simply reset (clear) the HSC Reset Bit and set the HSC Enable Bit. Note: if the HSC Enable Bit is still ON, you must reset (clear) this bit, and then set it again.

The following bits and registers are associated with the HSC:

Register/Bit	Description
Configuration Register	The 16-bit register that controls how the High-Speed counter operates.
Current Count Register	The 32-bit register that counts the number of times that the Trigger has transitioned. The specified register is the Least Significant Word (LSW); the next consecutive register is the Most Significant Word (MSW).
Preset Register	The 32-bit register that defines the number of counts at which the Done bit will be set (see description of Done Bit below). The specified register is the Least Significant Word (LSW); the next consecutive register is the Most Significant Word (MSW).
Trigger Bit	The input bit that triggers the count. The counter will increment by one on each bit transition. The counter can operate on a falling (default) or rising edge.
Enable Bit	The counter will not run unless this bit is set. If this bit is reset while the counter is running, the current values will be maintained, but the Trigger bit will have no effect. The Done bit is reset if the Enable bit is reset. If the Current Count value is greater than or equal to the Preset value, the Done bit is set after the Enable bit is set again.
Reset Bit	When this bit goes from false to true, the current count will reset to 0 and the Done bit is reset. The reset occurs even when the Enable bit is reset. The reset is accomplished by an internal bit or a physical input.
Done Bit	The physical output that turns on when the Current Count is equal to or greater than the Preset value. The bit remains set until the Reset bit goes true, even if the counter counts beyond the preset. If the Enable bit is reset, the Done bit will reset. If the Enable bit is set while the Current

	Count is equal to or greater than the Preset, the Done bit is set.

The following registers and I/O are associated with the HSC. For the register addresses listed below, nn stands for which slot the module was installed (slot 1 is 01, slot 2 02, etc.).

Function	Counter 1 (CH 0)	Counter 2 (CH 1)
Trigger Bit	Xnn000	Xnn002
Enable Bit	Mnn080	Mnn176
Reset Bit	Mnn081	Mnn177
Configuration Register	MWnn00	MWnn06
Current Count Register (LSW, MSW)	MWnn01, MWnn02	MWnn07, MWnn08
Preset Register (LSW, MSW)	MWnn03, MWnn04	MWnn09, MWnn10

For how to set the HSC Configuration Register, reference the tables below.

Input Mode	Output Mode	Register Value
Normal Input	N/A	0
High Speed, Single Phase, Up/Down Counter	Output ON when preset is reached	2
	Output ON when counter is enabled, OFF when preset is reached	258
Quadrature 4X	Output ON when preset is reached	131
	Output ON when counter is enabled, OFF when preset is reached	387

HSC Configuration Register Bit table:

Bits	Function
15-12	Not used
11-10	00: Reset counter if SW Reset bit or physical I/Preset bit goes from 0 to 1 01: Reset counter if the SW reset bit goes from 0 to 1 11: reserved for future use
9	Forced Output Configuration 0: Forced output ON for Preset 1 1: Forced output ON when enabled and OFF when Preset 1 reached
8	Forced Output Control 0: Forced Output Disabled 1: Forced Output Enabled
7-6	Quadrature mode 00: Reserved 01: Reserved 010: 4X Quadrature mode
4-5	HSC 00: Single Phase Up counter
3	0: Falling Edge 1: Rising Edge

2-0	Module Operating Mode 000: Normal Operation 010: Up Counter HSC 011: Quadrature

HMC7000 High Speed Counters

The HMC7000 Series products have built-in High-Speed counters that link directly to specific inputs and outputs. Specific registers and bits are predefined for setup and control of these counters. No logic is required to run the counters, other than logic that may be used to configure and control the counters.

Two inputs on the module are used as the Triggers for the High-Speed counters, and two outputs are used as the done bits. The inputs support a maximum speed of 25 KHz.

The following bits and registers are associated with a High-Speed counter:

Register/Bit	Description
Enable Bit	The counter will not run unless this bit is set. If this bit is reset while the counter is running, the current values will be maintained, but the trigger bit will have no effect. The done bit is reset. The reset occurs even when the enable bit is reset. If the current count value is greater than or equal to preset value, the done bit is set after the enable bit is set again.
Reset Bit	When the bit goes from false to true, the current count will reset to 0 and the done bit is reset. The reset occurs when the current is equal or greater than the preset value. The bit remains set until the reset bit goes true, even if the counter counts beyond the preset. If the enable bit is reset If the enable bit is set while the current count bit equal to the greater that the preset.
Done Bit	The physical output that turns on when the current count is equal to or greater than the preset value. The bit remains set until the reset button goes true, even if the counter counts beyond the preset. If the enable bit is reset, the done bit will reset. If the enable bit is set while the current count is equal to or greater than the preset, the done bit is set.
Configuration Register	The register that controls how the High-Speed counter operates.
Current Counter Register	The register that counts the number of times that the Trigger has transitioned. The specified register is the Least Significant Word (LSW); the next consecutive register is the Most Significant Word (MSW).
Preset Register	The register that defines the number of counts at which the Done bit will be set (see description of Done Bit above). The specified register is the Least Significant Word (LSW); the next consecutive register is the Most Significant Word (MSW).

For how to set the HSC Configuration Register, reference the tables below.

HSC Configuration Register values for the HMC7-MI-01, HMC7-MIO-02, HMC7-MIO-04, and HMC7030A-L:

Bits	Function
15-4	Not used
3	0: Falling Edge 1: Rising Edge

2-0	Module Operating Mode: 000: Normal Operation 010: Up Counter HSC

HSC Configuration Register values for the HMC7-MIO-04, HMC7-MIO-05, HMC7-MIO-06, and HMC7-MIO-07:

Input Mode	Output Mode	Register Value
Normal Mode	N/A	0
High Speed, Single Phase, Up Counter	Output ON when preset is reached	2
	Output ON when counter is enabled, OFF when preset is reached	258
Quadrature 1X	Output ON when preset is reached	3
	Output ON when counter is enabled, OFF when preset is reached	259
Quadrature 2X	Output ON when preset is reached	67
	Output ON when counter is enabled, OFF when preset is reached	323
Quadrature 4X	Output ON when preset is reached	131
	Output ON when counter is enabled, OFF when preset is reached	387

The following registers and I/O are associated with the HSC. For the register addresses listed below, nn stands for which slot the module was installed (slot 1 is 01, slot 2 02, etc.). Note that not all models have access to Channels 3 and 4. Consult the specifications for the particular model being used.

High Speed Counter Option	HSC CH1	HSC CH2	HSC CH3	HSC CH4
HSC Input	X0 (terminal) Xnn000 (register)	X5 (terminal) Xnn005 (register)	X2 (terminal) Xnn002 (register)	X7(terminal) Xnn007 (register)
HSC Reset Input	X1 (terminal) Xnn001 (register)	X6 (terminal) Xnn006 (register)	X3 (terminal) Xnn003 (register)	X4 (terminal) Xnn004 (register)
HSC Output Flag	Y1 (terminal) Ynn001 (register)	Y6 (terminal) Ynn006 (register)	Y7 (terminal) Ynn007 (register)	Y0 (terminal) Ynn000 (register)
HSC Configuration Register	MWnn00	MWnn06	MWn112	MWn118
HSC Counter Register (Current Value)	MWnn01 MWnn02	MWnn07 MWnn08	MWnn13 MWnn14	MWnn19 MWnn20
HSC Preset Register	MWnn03 MWnn04	MWnn09 MWnn10	MWnn15 MWnn16	MWnn21 MWnn22
HSC Enable Bit	Mnn080	Mnn176	Mnn272	Mnn368
HSC Reset Bit	Mnn081	Mnn177	Mnn273	Mnn369
Quadrature Inputs	**Pair 1**		**Pair 2**	

Counter Inputs	X0, X5	X2, X7
Counter Reset Input	X1	X3
Output Flag	Y1	Y7

MLC Series High Speed Counters

Many Maple Systems MLC products have built-in High-Speed Counters (HSCs) that link directly to specific inputs and outputs. Specific registers and bits are predefined for setup and control of these counters. No logic is required to run the counters, other than logic that may be used to configure and control the counters. Each HSC option on a given module is referred to as a 'channel', with a set of physical inputs/outputs and predefined tags. The number of channels supported depends upon the particular MLC product.

Implementation of HSC on MLC Series

1. Connect a device that will provide the high-speed pulses to one of the high-speed inputs on the expansion module.
2. Configure the HSC using the configuration register for that channel. Note: You can write to the configuration register value using the Power-Up logic block or in a Power-Up Task.
3. Write the HSC preset count value in that channel's Preset Register.
4. Enable the HSC by setting the HSC Enable Bit for that channel.
5. HSC increments the current value register for that channel until the preset value is reached.
6. Enable the HSC Reset Bit for that channel. This will cause the HSC current value to reset back to 0.
7. To start the process again, simply reset (clear) the HSC Reset Bit and set the HSC Enable Bit. Note: if the HSC Enable Bit is still ON, you must reset (clear) this bit, and then set it again.

The following bits and registers are associated with a High-Speed counter:

Register/Bit	Description
Enable Bit	The counter will not run unless this bit is set. If this bit is reset while the counter is running, the current values will be maintained, but the trigger bit will have no effect. The done bit is reset. The reset occurs even when the enable bit is reset. If the current count value is greater than or equal to preset value, the done bit is set after the enable bit is set again.
Reset Bit	When the bit goes from false to true, the current count will reset to 0 and the done bit is reset. The reset occurs when the current is equal or greater than the preset value. The bit remains set until the reset bit goes true, even if the counter counts beyond the preset. If the enable bit is reset If the enable bit is set while the current count bit equal to the greater that the preset.
Done Bit	The physical output that turns on when the current count is equal to or greater than the preset value. The bit remains set until the reset button goes true, even if the counter counts beyond the preset. If the enable bit is reset, the done bit will reset. If the enable bit is set while the current count is equal to or greater than the preset, the done bit is set.
Configuration Register	The register that controls how the High-Speed counter operates.
Current Counter Register	The register that counts the number of times that the Trigger has transitioned. The specified register is the Least Significant Word (LSW); the next consecutive register is the Most Significant Word (MSW).
Preset Register	The register that defines the number of counts at which the Done bit will be set (see description of Done Bit above). The specified register is the Least Significant Word (LSW); the next consecutive register is the Most Significant Word (MSW).

MLC Base Units with Built-in I/O (MLC1-F, MLC1-E, and MLC2-E models)

MLC1-F, MLC1-E, and MLC2-E base models support Single Phase Up, Single Phase Down, and Quadrature 4X modes at speeds of up to 200 kHz.

The following registers and I/O are associated with the MLC Base Unit HSC:

Function	Channel 1	Channel 2	IEC Data Type
Trigger Input or Encoder A	X0	X2	BOOL
Up/Down Input or Encoder B	X1	X3	BOOL
HW Reset Input	X4	X5	BOOL
Reset Bit (Internal)	M241	M721	BOOL
HW Done Output	Y2	Y3	BOOL
Preset Reached (Internal Done Bit)	M242	M722	BOOL
Enable Bit	M240	M720	BOOL
Configuration Register	MW10	MW40	WORD
Current Count Register (LSW, MSW)	MW11, MW12	MW41, MW42	DWORD
Preset Register (LSW, MSW)	MW13, MW14	MW43, MW44	DWORD

HSC Configuration Register values for MLC Base units:

Input Mode	Output Mode	Register Value
Normal Input (HSC not enabled)	N/A	0
High-Speed Single Phase Counter, Up or Down based on Up/Down Input	HW Done Bit Disabled	2
	HW Done output ON when preset is reached	258
	Done output ON when counter is enabled, OFF when preset is reached	770
Quadrature 4X	HW Done Bit Disabled	131
	HW Done output ON when preset is reached	387
	Done output ON when counter is enabled, OFF when preset is reached	899

High-Speed Expansion Modules (MLE-0808NH, MLE-0808PH)

The MLE-0808NH and MLE-0808PH expansion modules support four Single Phase Up counters at speeds of up to 25kHz or two Quadrature counters in 1X, 2X, or 4X modes at speeds of up to 5kHz on Channel 1 or 20kHz on Channel 2. If both channels are used simultaneously in quadrature mode, the max speed is 5kHz for both.

The following registers and I/O are associated with the MLC Expansion Modules HSC:

Function	Channel 1	Channel 2	Channel 3	Channel 4	IEC Data Type
Trigger Input (Single Phase)	Xnn000	Xnn005	Xnn002	Xnn007	BOOL
Encoder A (Quadrature)	Xnn000	N/A	Xnn002	N/A	BOOL
Encoder B (Quadrature)	Xnn005	N/A	Xnn007	N/A	BOOL
HW Reset Input (Single Phase)	Xnn001	Xnn006	Xnn003	Xnn004	BOOL
HW Reset Input (Quadrature)	Xnn001	N/A	Xnn003	N/A	BOOL
Reset Bit (Internal)	Mnn209	Mnn273	Mnn337	Mnn401	BOOL
Done Output (Single Phase)	Ynn001	Ynn006	Ynn007	Ynn000	BOOL
Done Output (Quadrature)	Ynn001	N/A	Ynn007	N/A	BOOL
Preset Reached (Internal Done Bit)	Xnn048	Xnn049	Xnn050	Xnn051	BOOL
Enable Bit	Mnn208	Mnn272	Mnn336	Mnn400	BOOL
Configuration Register	MWnn10	MWnn14	MWnn18	MWnn22	WORD
Preset Register (LSW, MSW)	MWnn11, MWnn12	MWnn15, MWnn16	MWnn19, MWnn20	MWnn23, MWnn24	DWORD
Count Register (LSW, MSW)	XWnn04, XWnn05	XWnn06, XWnn07	XWnn08, XWnn09	XWnn10 XWnn11	DWORD

HSC Configuration Register values for MLC Expansion Modules:

Input Mode	Output Mode	Register Value
Normal Input (HSC not enabled)	N/A	0
High-Speed Single Phase UP Counter	HW Done output ON when preset is reached	2
	HW Done output ON when counter is enabled, OFF when preset is reached	258
Quadrature 1X	HW Done output ON when preset is reached	3
	HW Done output ON when counter is enabled, OFF when preset is reached	259
Quadrature 2X	HW Done output ON when preset is reached	67
	HW Done output ON when counter is enabled, OFF when preset is reached	323
Quadrature 4X	HW Done output ON when preset is reached	131
	HW Done output ON when counter is enabled, OFF when preset is reached	387

High-Speed Counter Operation to implement High-Speed Counter Operation (using a MLC CPU base module as example):

1. Connect a device to X0 (Channel 1) or X2 (Channel 2) that will provide the high-speed pulses to the expansion module.

2. Configure for HSC mode using the configuration register MW0010 (Channel1) or MW0040 (Channel2)

3. Write the HSC preset count value in MW0013 (Channel 1) or MW0043 (Channel 2).

4. Enable the HSC by setting the HSC Enable Bit M00240 (Channel 1) or M00720 (Channel 2).

5. HSC increments (starting from 0) or decrements (starting from 4,294,967,295) the current value register in MW0011 (Channel 1) or MW0041 (Channel 2) until the preset value is reached. Then HSC sets Y2 (Channel 1) or Y3 (Channel 2).

6. Enable the HSC Reset Bit by setting M00241 (Channel 1) or M00721 (Channel 2). Or by setting Reset Pin X4 (Channel 1) or Reset Pin X5 (Channel 2). This will cause the HSC current value to reset back to 0 and the output Y2 (Channel 1) or output Y3 (Channel 2) will reset (clear) to 0. MLC PLC Series I/O Module Guide 24 MLC PLC Series I/O Module Guide 24

7. To start the process again, simply reset (clear) the HSC Reset Bit and set the HSC Enable Bit. Note: If the HSC Enable Bit is still ON, you must reset (clear) this bit, and then set it again.